An Instrumentation Approach for Hardware-Agnostic Software Characterization

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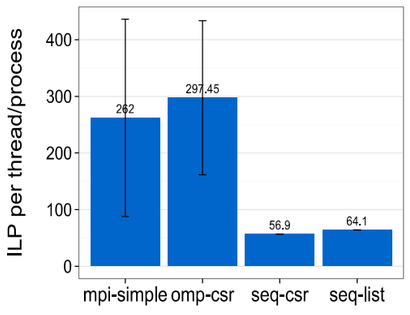
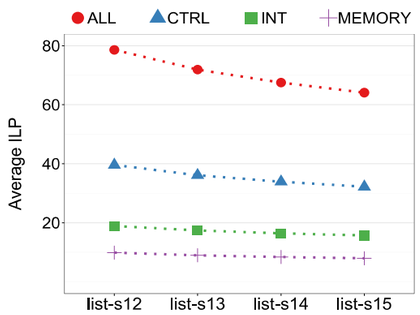
Simulators and empirical profiling data are often used to understand how suitable a specific hardware architecture is for an application. However, simulators can be slow, and empirical profiling-based methods can only provide insights about the existing hardware on which the applications are executed.

We introduce an alternative to these approaches: we propose a framework based on the **LLVM compiler infrastructure** that is capable of analyzing, in a hardware-agnostic manner, the inherent instruction-level parallelism and memory access patterns in sequential and parallel applications. We provide a detailed characterization of a representative benchmark for graph-based analytics, Graph 500, by providing an analysis of the intrinsic properties of various implementations of the benchmark.

ILP – ideal machine model

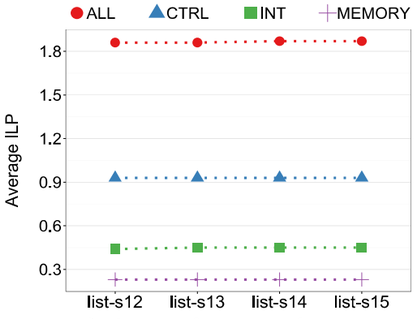


a) graph500-s15

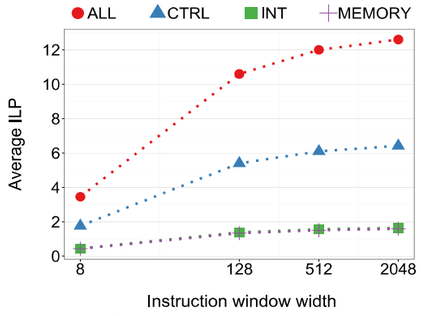


b) seq-list

ILP – ideal machine with hardware constrains



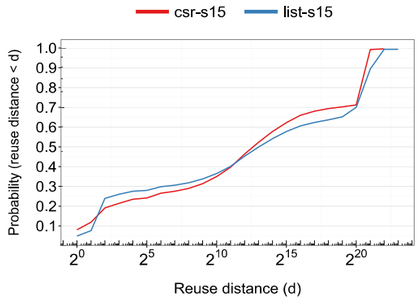
a) CTRL instructions serialized



b) limited instruction window

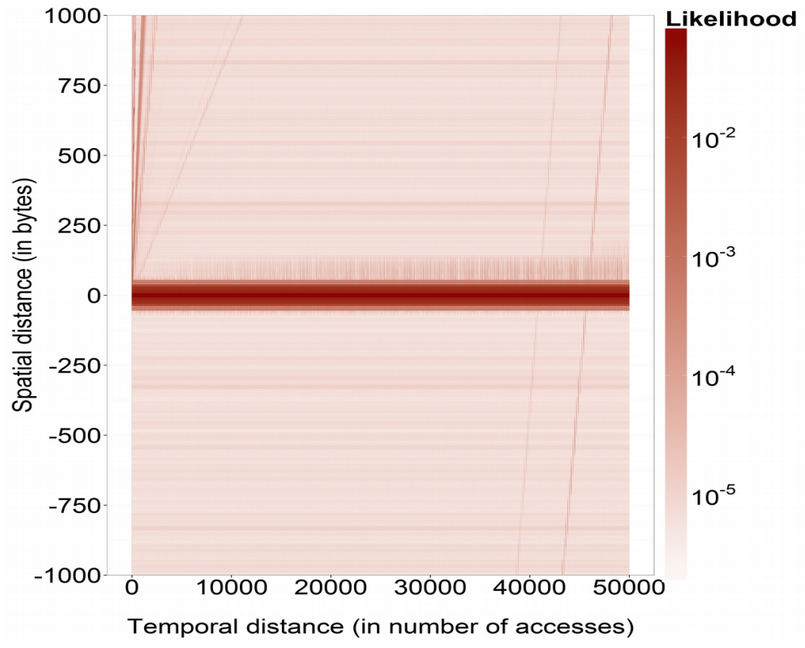
Data Temporal Reuse distribution

a) seq-list



b) seq-list vs. seq-csr

Memory access patterns



This work has been developed at IBM Research Zurich.