University
POLITEHNICA
of Bucharest

Faculty of
Automatic Control
and Computers

Computer Science
and Engineering
Department

Compiler for Vector Processing and Frequency Scaling at Instruction Level

Master Project – September 2014

Author

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biology

Computer Vision

biology

+

mathematics

Computer Vision

biology

+

mathematics

+

algorithms design

Computer Vision

biology

+

mathematics

+

algorithms design

+

hardware design

Computer Vision

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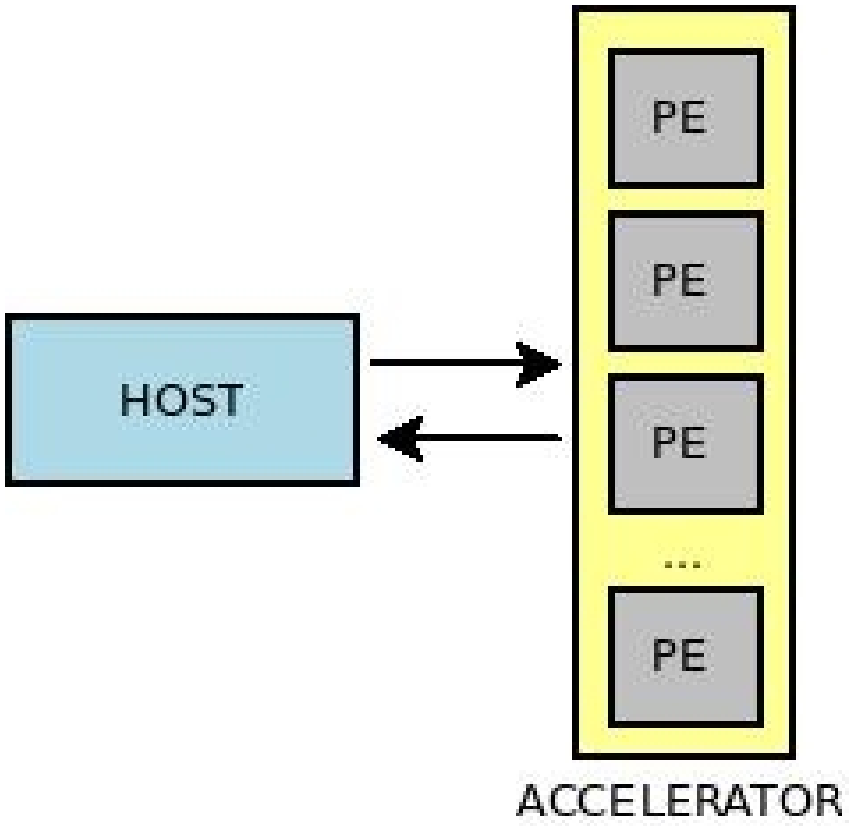
hardware design



Starting Point

ConnexArray – architecture designed for computer vision applications

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- development process: **heavy**

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  - specific assembly

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ConnexArray – architecture designed for computer vision applications

- development process: **heavy**
  - specific assembly
  - rewrite any application

Objectives

- run computer vision applications

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- run computer vision applications
- write applications in an architecture independent programming language

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- run computer vision applications
- write applications in an architecture independent programming language
- optimize the running process

Solution

- **Compiler for ConnexArray**

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  - modularity

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  - easy to extend

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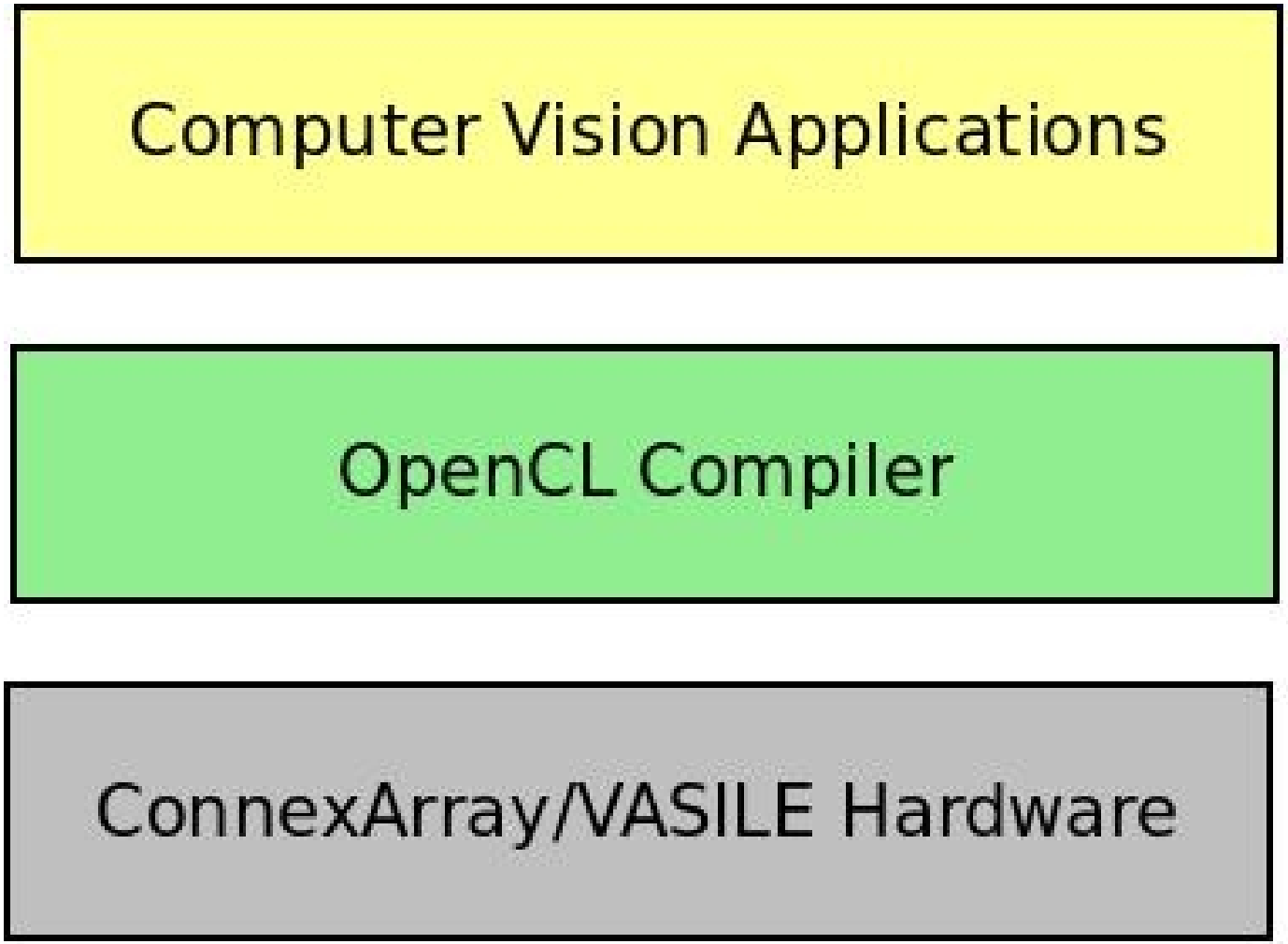
Solution

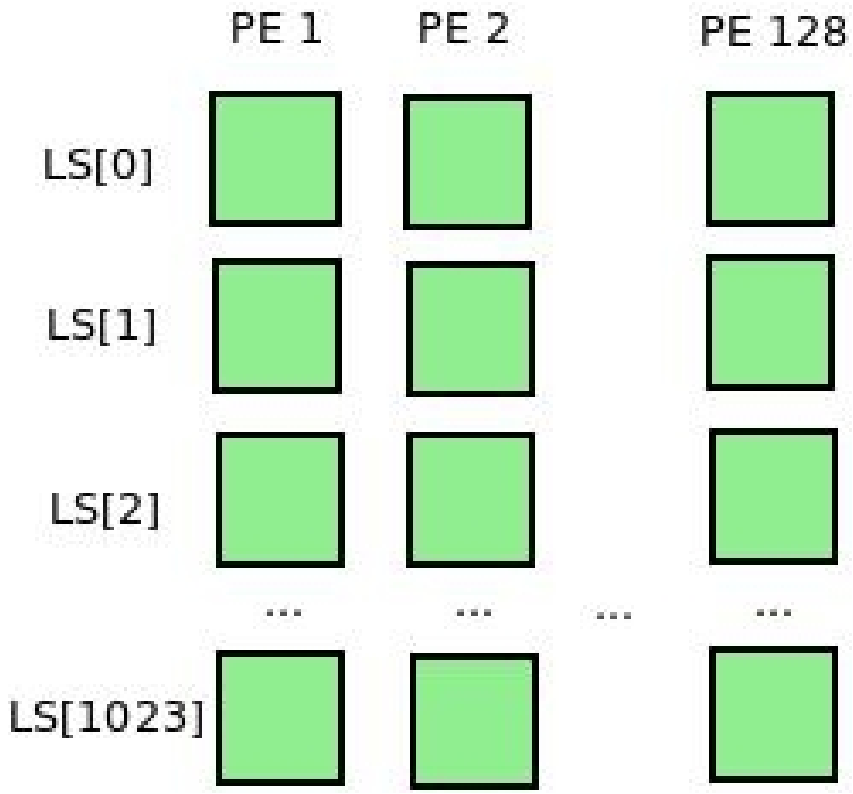
- **Compiler for ConnexArray**
  - modularity
  - easy to extend
  - no hard-constraints for a programming language
  - frequency scaling at instruction level (***VASILE***)

Overview


Computer Vision Applications
OpenCL Compiler
ConnexArray/VASILE Hardware

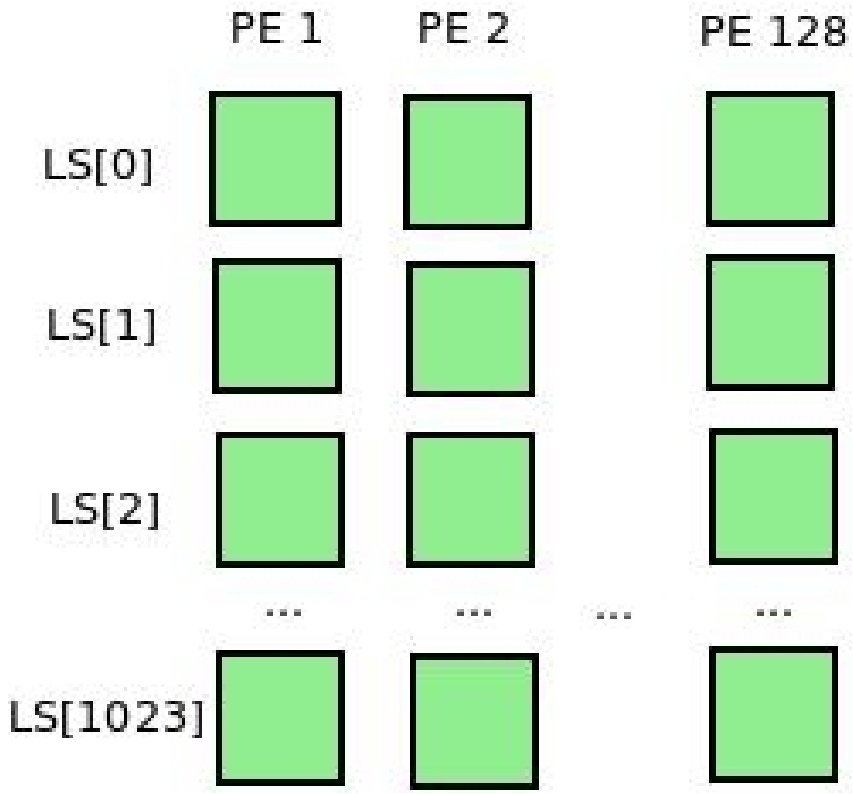
ConnexArray Architecture

- SIMD architecture



ConnexArray Architecture

- SIMD architecture
- 128 execution units



ConnexArray Architecture

- SIMD architecture
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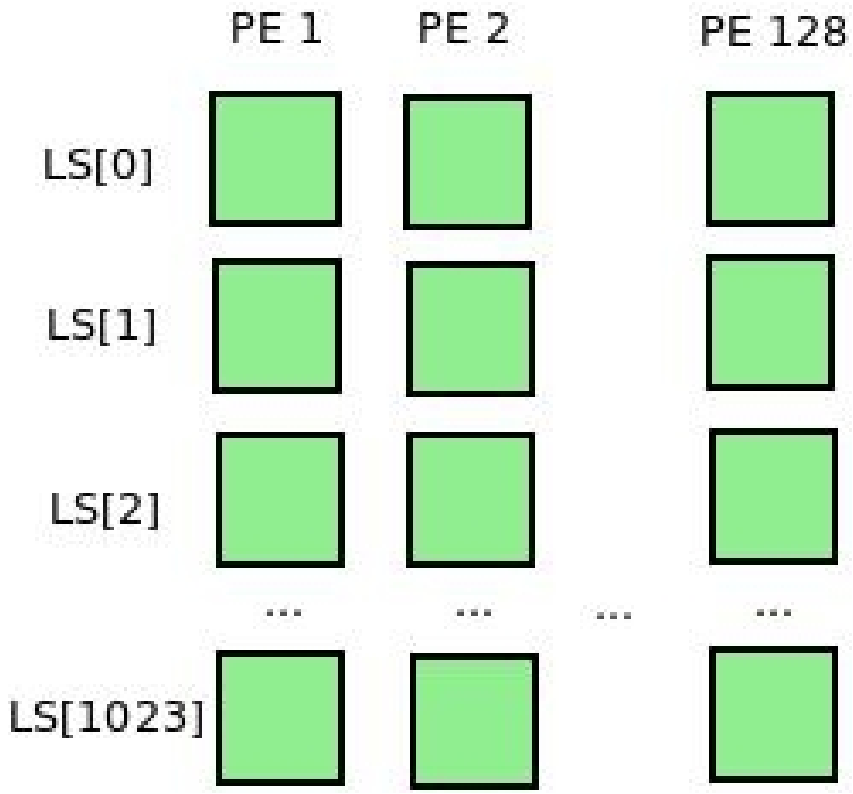

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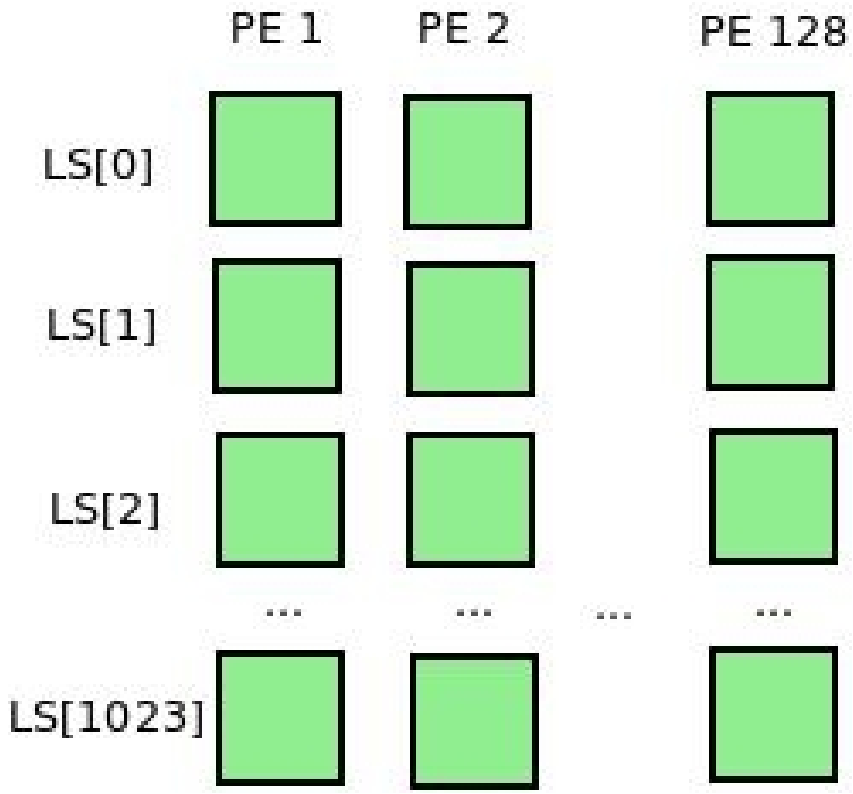

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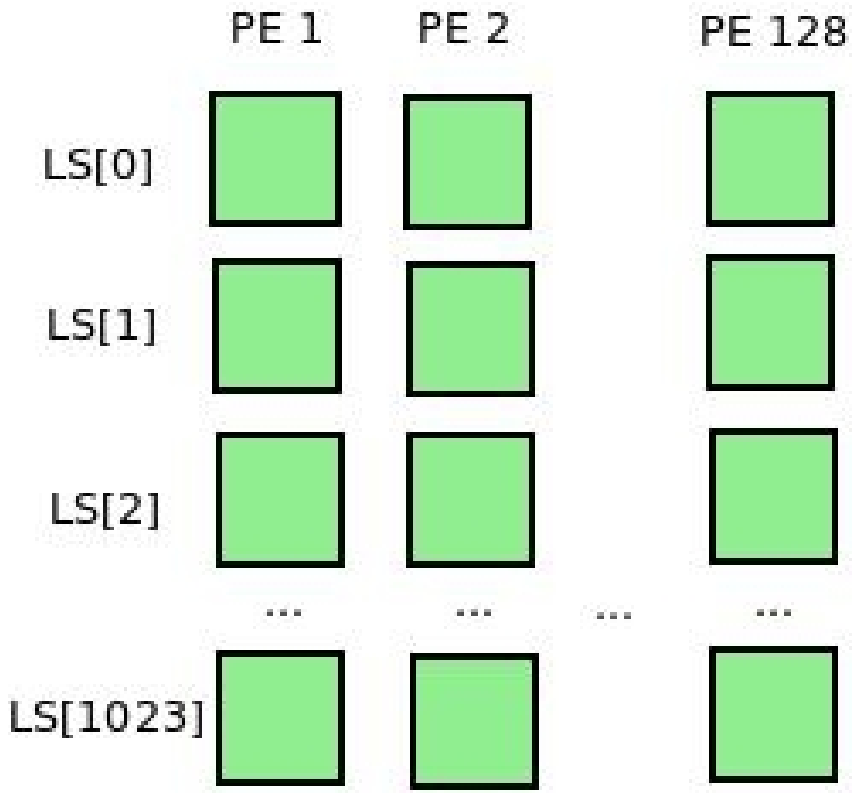

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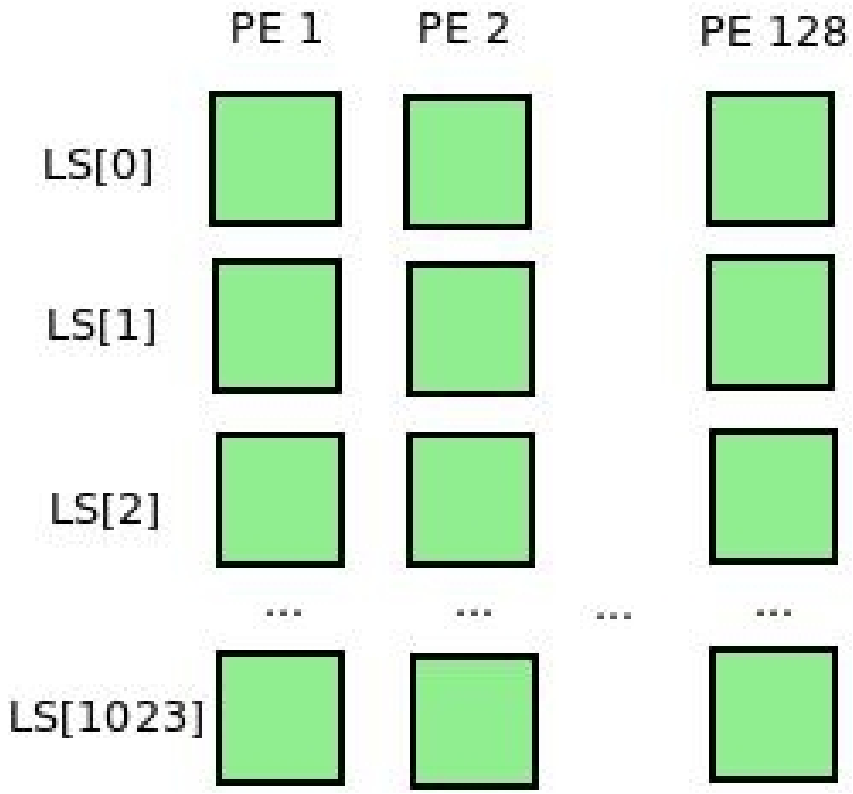
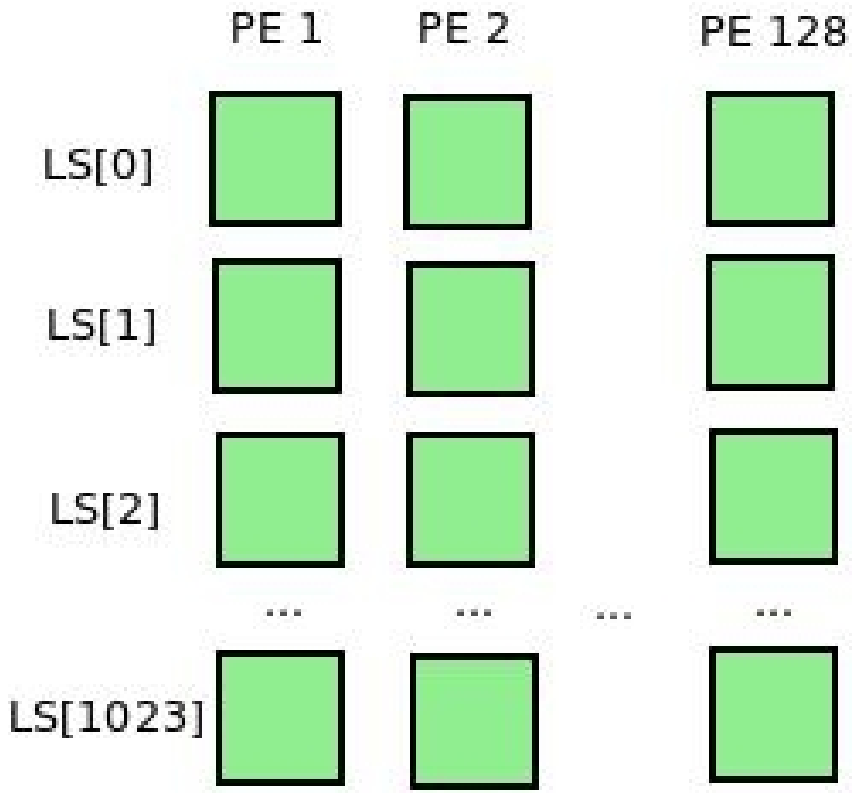
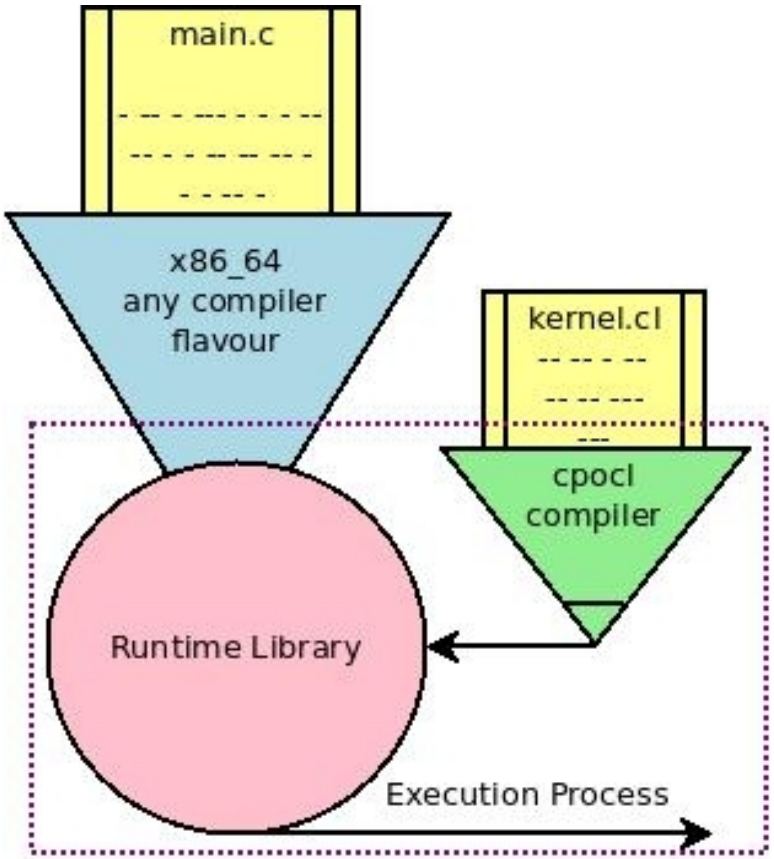


ConnexArray Architecture

- SIMD architecture
- 128 execution units
- implemented in FPGA
- custom ISA
- no control instructions
- Local Store: 1024 cells
- memory:
  128 x 1024 x 2

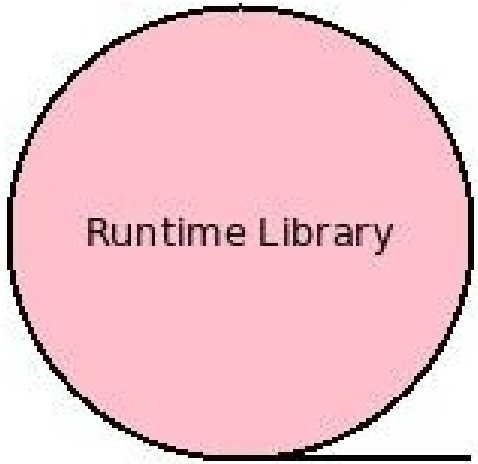


OpenCL Compiler Infrastructure



Runtime Library

- implements OpenCL standard API



Runtime Library

- implements OpenCL standard API
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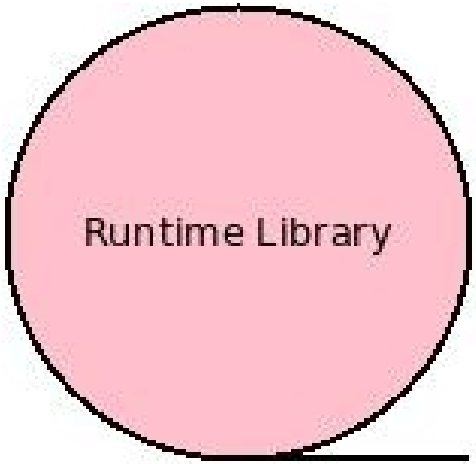
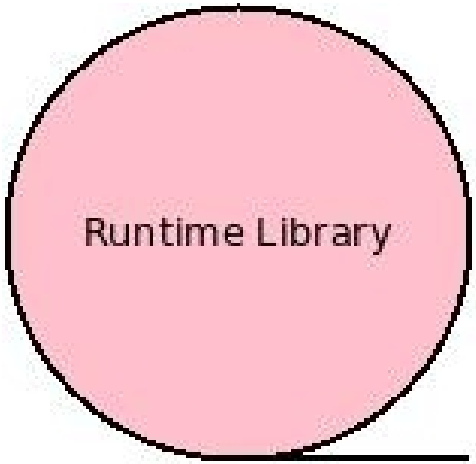


Runtime Library

- implements OpenCL standard API

- memory management
- data transfers



Runtime Library

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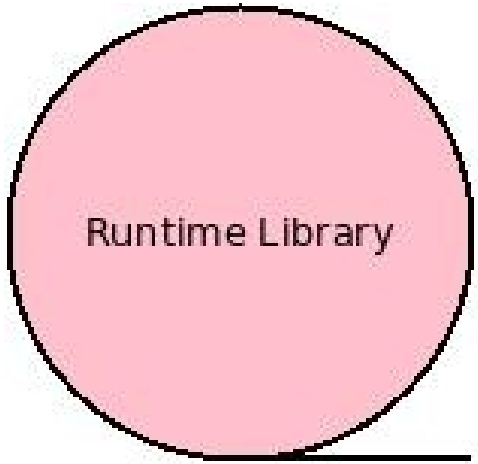
- handles runtime compilation



Runtime Library

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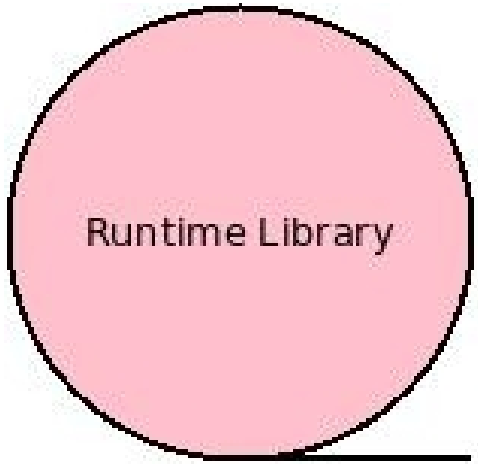
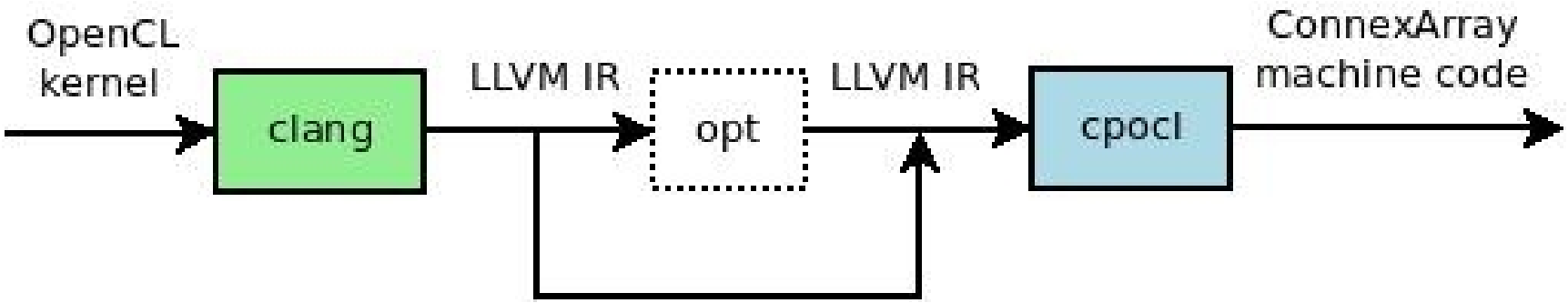
- handles execution flow



cpocl – ConnexArray CodeGen



VASILE optimization

- **V**ector **A**rchitecture for frequency **S**caling at **I**nstruction **LE**vel
  - ConnexArray enhancement

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Steps:

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- compiler configuration – loop tiling

Hardware Profiling

SSD algorithm: $\sum(a_i - b_i)^2$

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Instructions	Max. Freq. (Mhz)	Coverage
Addition/Substraction	160	54 %
Multiplication/Division	117	34 %
Memory Access	160	12 %

VASILE optimization - results

SSD algorithm: $\sum(a_i - b_i)^2$

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	Time (s)
ConnexArray	1.397
VASILE	1.186

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Keywords: computer vision, ConnexArray, compiler, frequency scaling

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